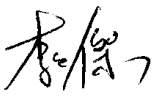
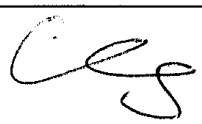
DOCUMENT NUMBER AND REVISION

VL-FS-COG-BT120032-01 REV. A

(COG-BT120032AVB-STF-12-LED02YG)

DOCUMENT TITLE:

SPECIFICATION
OF
LCD MODULE TYPE
ITEM NO.: COG-BT120032-01

DEPARTMENT	NAME	SIGNATURE	DATE
PREPARED BY	PHILIP CHENG		2002.05.13
CHECKED BY	TOM LEE		2002.05.13
APPROVED BY	CYRUS CHEUNG		2002.05.13

DOCUMENT REVISION HISTORY 1:

DOCUMENT REVISION FROM TO	DATE	DESCRIPTION	CHANGED BY	CHECKED BY
A	2002.05.13	First Release. (Reference:VL-FS-COG-LCM075-02,REV. A, 2001.12.14; VL-TS-COG-BT120032-01,REV. A,2002.02.06)	PHILIP CHENG	TOM LEE

CONTENTS

Specification
of
LCD Module Type
Item No.: COG-BT120032-01

1. General Description

- 120x 32 dots STN Postive Yellow Transflective Dot Matrix LCD Module.
- Viewing Angle: 12 o'clock direction.
- Driving duty: 1/33 duty, 1/6 bias.
- 'Seiko Epson' SED1567D0B (COG) Dot Matrix LCD Driver.
- 8080 Series MPU interface.
- Parallel data input.
- Yellow-green LED02 backlight.
- FPC.

2. Mechanical Specifications

The mechanical detail is shown in Fig. 1 and summarized in Table 1 below.

Table 1

Parameter	Specifications	Unit
Outline dimensions	66.6(W) x 92.8(H) x 5.0(D) (Module) 65.8(W) x 29.0(H) x 2.8(D) (LCD)	mm
Effective viewing area	60.0(W) x 16.0(H)	mm
Active area	57.55(W) x 13.71(H)	mm
Display format	120 (W) x 32(H)	dots
Dot size	0.43(W) x 0.38(H)	mm
Dot spacing	0.05(W) x 0.05(H)	mm
Dot pitch	0.48(W) x 0.43(H)	mm
Weight:	TBD	grams

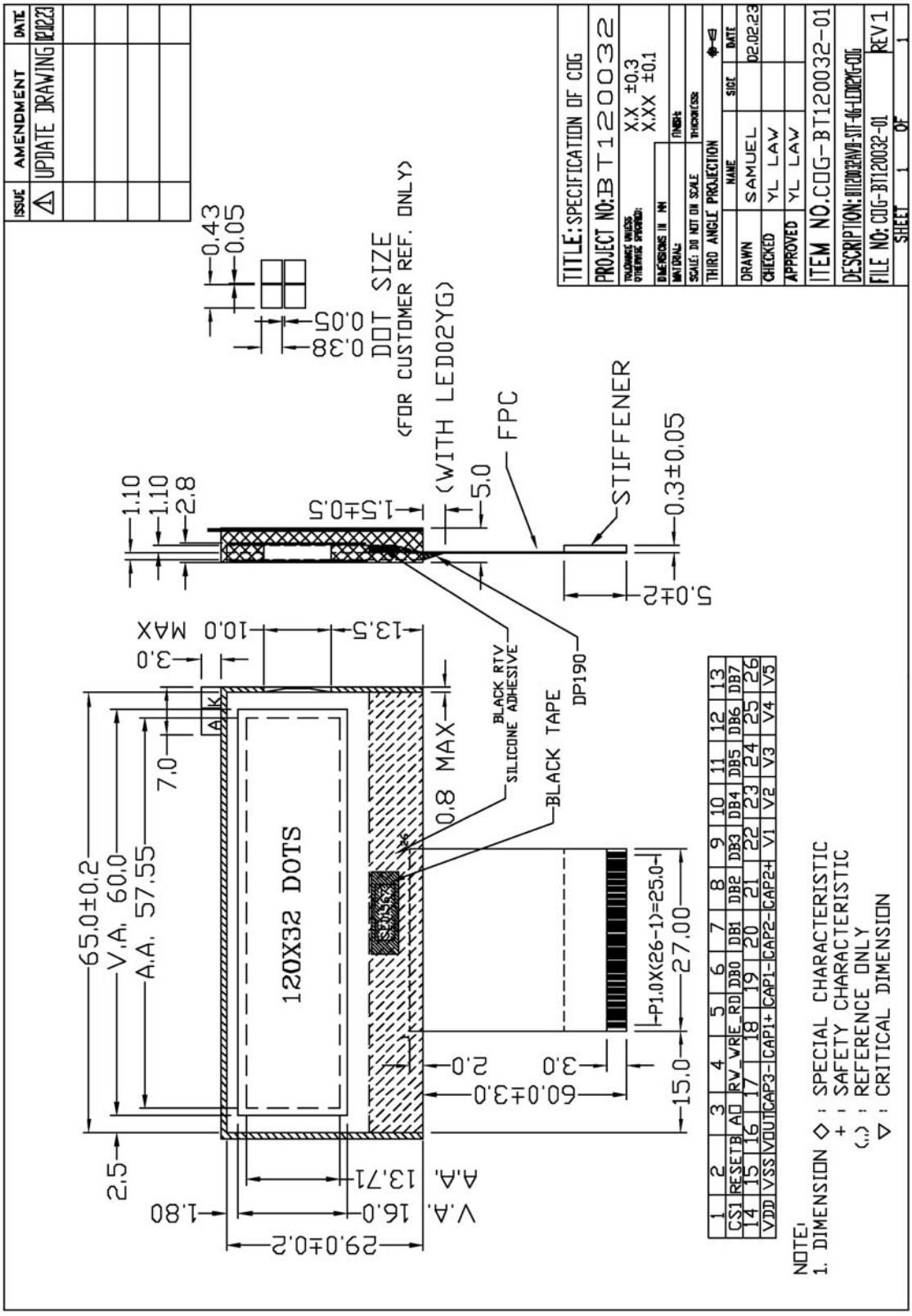


Figure 1: Specification of the COG-BT120032-01 module.

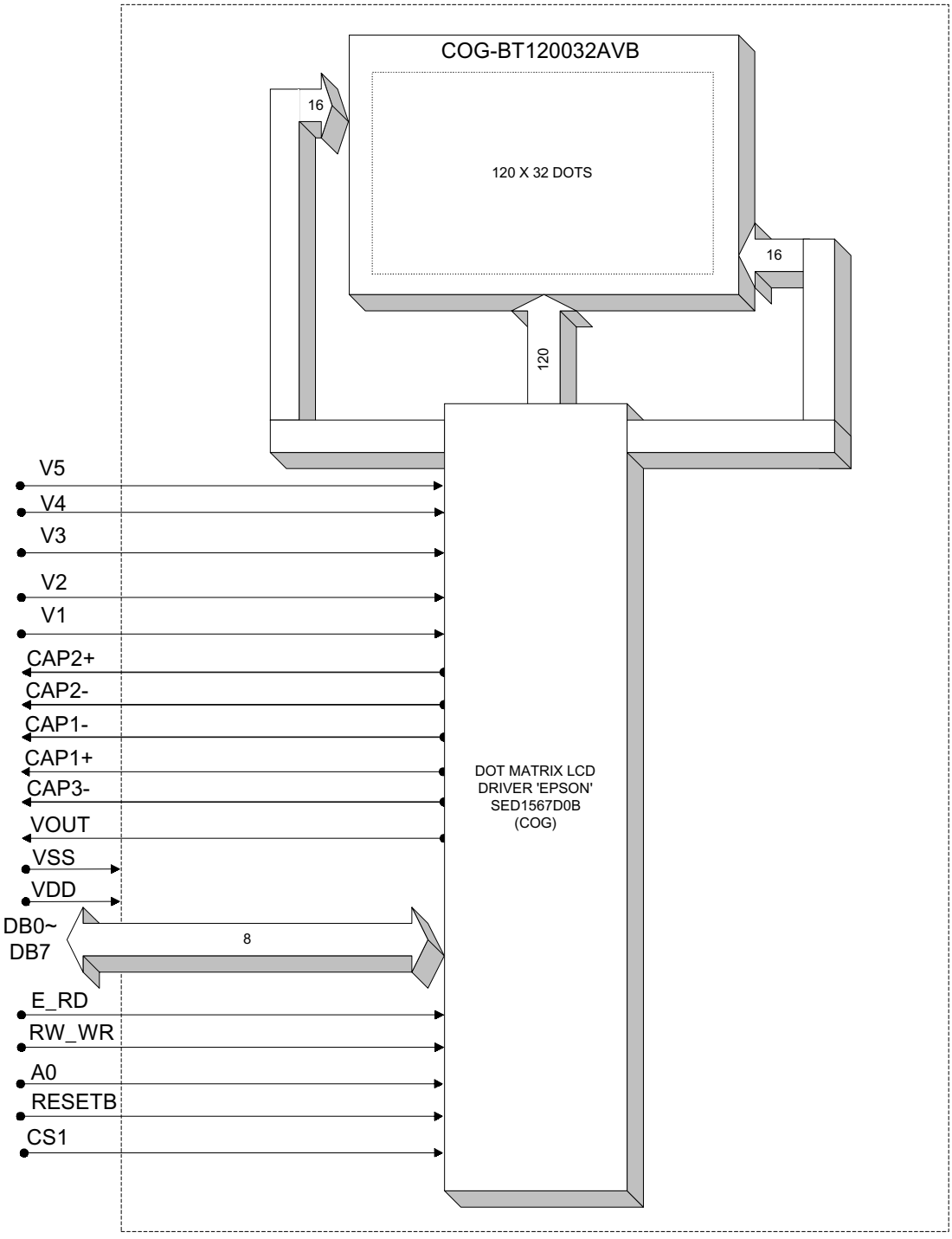


Figure 2: Block Diagram

3. Interface signals

Table 2(a)

Pin No.	Symbol	Description
1	CS1	This is the chip select signal. When CS1 = "L", then the chip select become active, and data/command I/O is enabled.
2	RESETB	When RESETB is set to "L," the settings are initialized. The reset operation is performed by the RESETB signal level.
3	A0	This is connected to the least significant bit of the normal MPU address bus, and it determines whether the data bits are data or a command. A0 = "H": Indicates that DB0 to DB7 are display data. A0 = "L": Indicates that DB0 to DB7 are control data.
4	RW_WR	• When connected to an 8080 MPU, this is active LOW. This terminal connects to the 8080 MPU WR signal. The signals on the data bus are latched at the rising edge of the WR signal.
5	E_RD	• When connected to an 8080 MPU, this is active LOW. This pin is connected to the RD signal of the 8080 MPU, and the SED1565 series data bus is in an output status when this signal is "L".
6	DB0	This is an 8-bit bi-directional data bus that connects to an 8-bit or 16-bit 8 standard MPU data bus.
7	DB1	
8	DB2	
9	DB3	
10	DB4	
11	DB5	
12	DB6	
13	DB7	
14	VDD	Power supply for logic (+3V).
15	VSS	Ground (0V)

Table 2(b)

Pin No.	Symbol	Description
16	VOUT	DC/DC voltage converter. Connect a capacitor between this terminal and VSS
17	CAP3-	DC/DC voltage converter. Connect a capacitor between this terminal and the CAP1+ terminal.
18	CAP1+	DC/DC voltage converter. Connect a capacitor between this terminal and the CAP1- terminal.
19	CAP1-	DC/DC voltage converter. Connect a capacitor between this terminal and the CAP1+ terminal.
20	CAP2-	DC/DC voltage converter. Connect a capacitor between this terminal and the CAP2+ terminal.
21	CAP2+	DC/DC voltage converter. Connect a capacitor between this terminal and the CAP2- terminal.
22	V1	This is a multi-level power supply for the liquid crystal drive. The voltage applied is determined by the liquid crystal cell, and is changed through the use of a resistive voltage divided or through changing the impedance using an op. amp. Voltage levels are determined based on VDD, and must maintain the relative magnitudes shown below. VDD (= V0)≧V1 ≧V2 ≧V3 ≧V4 ≧V5 Master operation: When the power supply turns ON, the internal power supply circuits produce the V1 to V4 voltages shown below. The voltage settings are selected using the LCD bias set command. For 1/6 bias: V1=(1/6)xV5, V2=(2/6)xV5, V3=(4/6)xV5, V4=(5/6)xV5.
23	V2	
24	V3	
25	V4	
26	V5	

4. Absolute Maximum Ratings

4.1 Electrical Maximum Ratings(Ta = 25 ºC)

Table 3

Parameter	Symbol	Conditions	Min.	Max.	Unit
Power Supply voltage (Logic)	VDD – VSS		-0.3	+7.0	V
Input voltage	Vin		-0.3	VDD+0.3	V
Power Supply voltage(2)	VSS2		-7.0	+0.3	V
		With Triple step-up	-6.0	+0.3	V
		With Quad step-up	-4.5	+0.3	V
Power Supply voltage(3)	V5,VOUT		-18.0	+0.3	V
Power Supply voltage(4)	V1,V2,V3,V4		V5	+0.3	V

Note:

1.)The modules may be destroyed if they are used beyond the absolute maximum ratings.

2.)All voltage values are referenced to VSS= 0V.

3.) Insure that the voltage levels of V1, V2, V3,and V4 are always such that
VDD ≧V1 ≧V2 ≧V3 ≧V4 ≧V5.

4.2 Environmental Condition

Table 4

Item	Operating Temperature (Topr)		Storage Temperature (Tstg)		Remark
	Min.	Max.	Min.	Max.	
Ambient Temperature	0°C	+50°C	-20°C	+60°C	Dry
Humidity	95% max. RH for Ta ≤ 40°C < 95% RH for Ta > 40°C				no condensation
Vibration (IEC 68-2-6) cells must be mounted on a suitable connector	Frequency: 10 ~ 55 Hz Amplitude: 0.75 mm Duration: 20 cycles in each direction.				3 directions
Shock (IEC 68-2-27) Half-sine pulse shape	Pulse duration : 11 ms Peak acceleration: 981 m/s^2 = 100g Number of shocks : 3 shocks in 3 mutually perpendicular axes.				3 directions

5. Electrical Specifications

5.1 Typical Electrical Characteristics

At Ta = 25 °C, VDD = 3V±0.2V, VSS=0V.

Table 5

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply voltage (Logic)	VDD-VSS		2.8	3.0	3.2	V
Supply voltage (LCD)	VLCD =VDD-V5	VDD = +3.0V, Note 1	6.2	6.5	6.8	V
Low-level input signal voltage	V_{ILC}		VSS	-	0.2xVDD	V
High-level input signal voltage	V_{IHC}		0.8xVDD	-	VDD	V
Supply Current (Logic & LCD)	IDD	Character mode, VDD = +3.0V	-	163	213.5	µA
		Checker board mode,VDD = +3.0V	-	261	302	µA
Supply voltage of yellow-green LED02 backlight		Number of LED chips=2x5=10. Forward current =75mA.	4.0	4.1	4.2	V

Note (1) : There is tolerance in optimum LCD driving voltage during production and it will be within the specified range.

5.2 Timing Specifications

Reset Timing

At Ta = 0 °C to +50 °C, VDD = +3V±0.2V, VSS = 0V.

Table 6

Item	Signal	Symbol	Condition	Rating			Units
				Min	Typ	Max	
Reset time		tR		—	—	1	µs
Reset "L" pulse width	RES	tRW		1	—	—	µs

Note :All timing is specified with 20% and 80% of VDD as the standard.

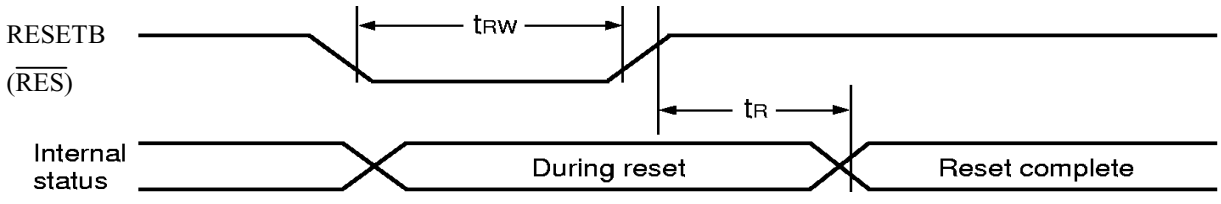


Figure 3:Reset Timing

System Bus Read/Write Characteristics (For the 8080 Series MPU)

At Ta = 0 °C to +50 °C, VDD = +3V±0.2V, VSS = 0V.

Table 7

Item	Signal	Symbol	Condition	Rating		Units
				Min	Max	
Address hold time	A0	t_{AH8}		0	—	ns
Address setup time		t_{AW8}		0	—	ns
System cycle time	A0	t_{CYC8}		300	—	ns
Control L pulse width ($\overline{WR}$)	$\overline{WR}$	t_{CCLW}		60	—	ns
Control L pulse width ($\overline{RD}$)	$\overline{RD}$	t_{CCLR}		120	—	ns
Control H pulse width ($\overline{WR}$)	$\overline{WR}$	t_{CCHW}		60	—	ns
Control H pulse width ($\overline{RD}$)	$\overline{RD}$	t_{CCHR}		60	—	ns
Data setup time	D0 to D7	t_{DS8}		40	—	ns
Address hold time		t_{DH8}		15	—	ns
$\overline{RD}$ access time		t_{ACC8}	C_L = 100 pF	—	140	ns
Output disable time		t_{OH8}		10	100	ns

*1 The input signal rise time and fall time (t_r, t_f) is specified at 15 ns or less. When the system cycle time is extremely fast, ($t_r + t_f$) ≤ ($t_{CYC8} – t_{CCLW} – t_{CCHW}$) for ($t_r + t_f$) ≤ ($t_{CYC8} – t_{CCLR} – t_{CCHR}$) are specified.
*2 All timing is specified using 20% and 80% of V_{DD} as the reference.
*3 t_{CCLW} and t_{CCLR} are specified as the overlap between $\overline{CS1}$ being "L" (CS2 = "H") and $\overline{WR}$ and $\overline{RD}$ being at the "L" level.

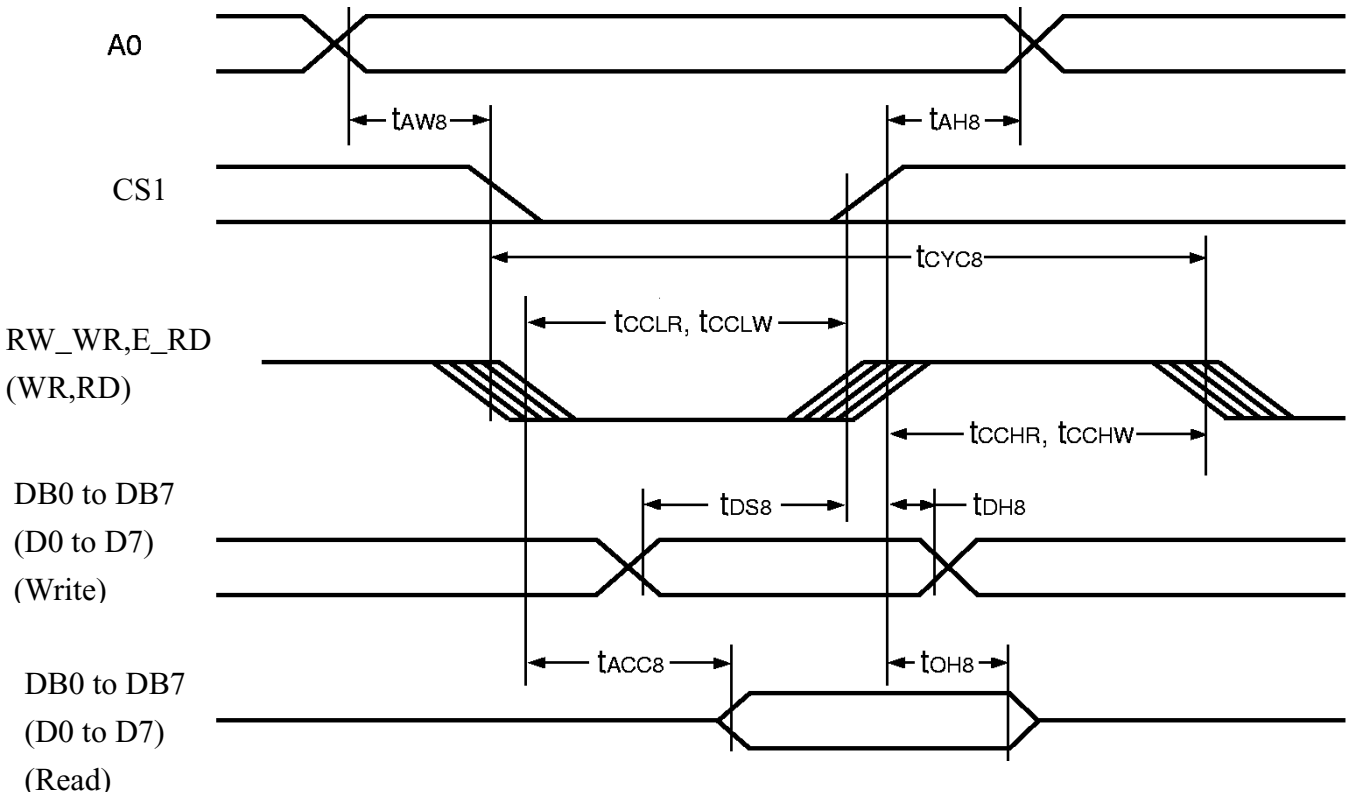


Figure 4: MPU bus read / write timing diagram (80 family MPU)

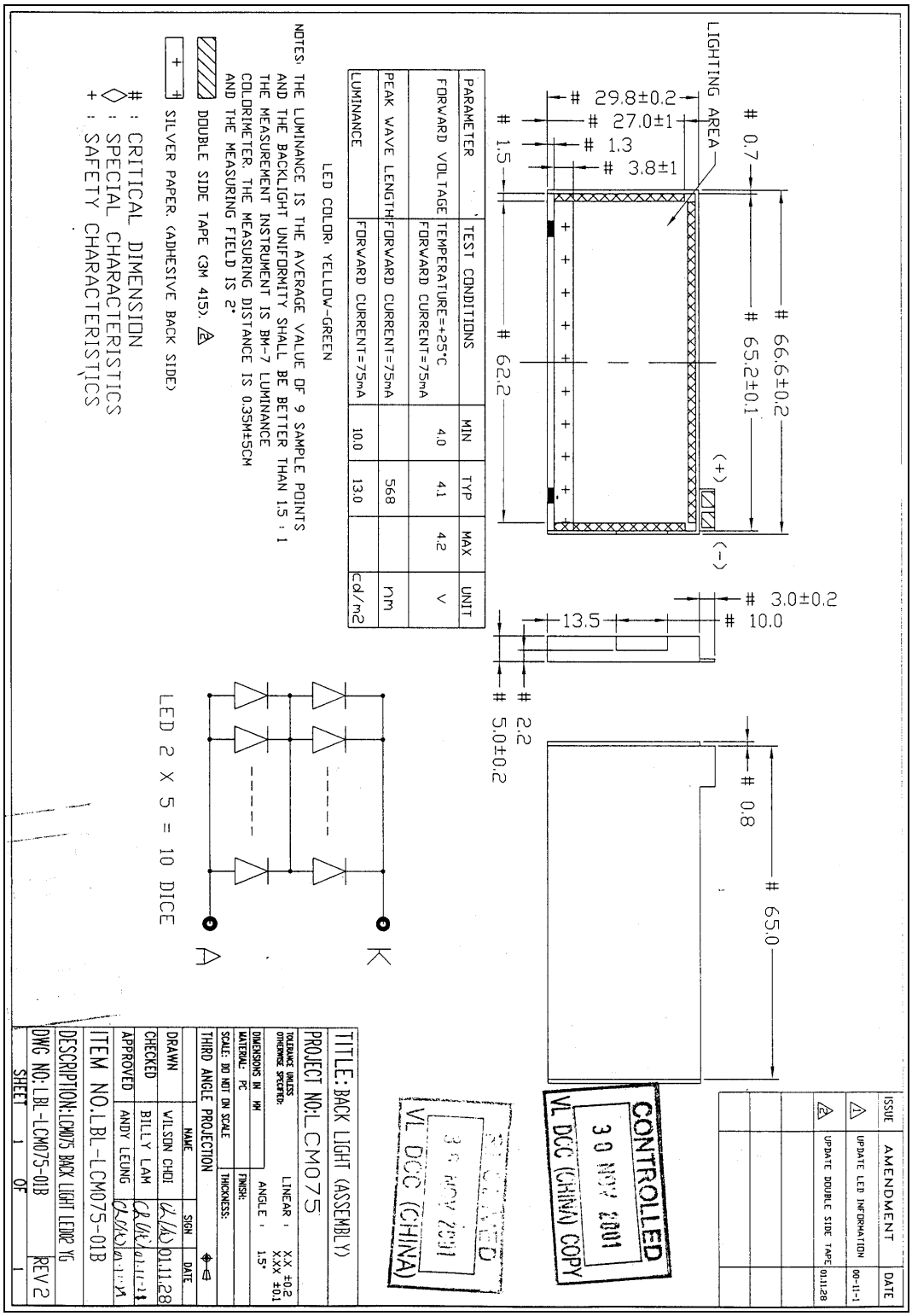
5.3 Instruction Set

Table 8

	Command	Command Code A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	Function
(1)	Display ON/OFF	0	1	0	1	0	1	0	1	1	1	0 1	LCD display ON/OFF 0: OFF, 1: ON
(2)	Display start line set	0	1	0	0	1	Display start address						Sets the display RAM display start line address
(3)	Page address set	0	1	0	1	0	1	1	Page address				Sets the display RAM page address
(4)	Column address set upper bit	0	1	0	0	0	0	1	Most significant column address				Sets the most significant 4 bits of the display RAM column address.
	Column address set lower bit	0	1	0	0	0	0	0	Least significant column address				Sets the least significant 4 bits of the display RAM column address.
(5)	Status read	0	0	1	Status				0	0	0	0	Reads the status data
(6)	Display data write	1	1	0	Write data								Writes to the display RAM
(7)	Display data read	1	0	1	Read data								Reads from the display RAM
(8)	ADC select	0	1	0	1	0	1	0	0	0	0	0 1	Sets the display RAM address SEG output correspondence 0: normal, 1: reverse
(9)	Display normal/ reverse	0	1	0	1	0	1	0	0	1	1	0 1	Sets the LCD display normal/ reverse 0: normal, 1: reverse
(10)	Display all points ON/OFF	0	1	0	1	0	1	0	0	1	0	0 1	Display all points 0: normal display 1: all points ON
(11)	LCD bias set	0	1	0	1	0	1	0	0	0	1	0 1	Sets the LCD drive voltage bias ratio SED1565*** ..... 0: 1/9, 1: 1/7 SED1566*** /SED1568*** /SED1569*** ..... 0: 1/8, 1: 1/6 SED1567*** 0: 1/6, 1: 1/5
(12)	Read/modify/write	0	1	0	1	1	1	0	0	0	0	0	Column address increment At write: +1 At read: 0
(13)	End	0	1	0	1	1	1	0	1	1	1	0	Clear read/modify/write
(14)	Reset	0	1	0	1	1	1	0	0	0	1	0	Internal reset
(15)	Common output mode select	0	1	0	1	1	0	0	0 1	*	*	*	Select COM output scan direction 0: normal direction, 1: reverse direction
(16)	Power control set	0	1	0	0	0	1	0	1	Operating mode			Select internal power supply operating mode
(17)	V_5 voltage regulator internal resistor ratio set	0	1	0	0	0	1	0	0	Resistor ratio			Select internal resistor ratio (Rb/Ra) mode
(18)	Electronic volume mode set	0	1	0	1	0	0	0	0	0	0	1	
	Electronic volume register set	0	1	0	*	*	Electronic volume value						Set the V_5 output voltage electronic volume register
(19)	Static indicator ON/OFF	0	1	0	1	0	1	0	1	1	0	0 1	0: OFF, 1: ON
	Static indicator register set	0	1	0	*	*	*	*	*	*	Mode		Set the flashing mode
(20)	Power saver												Display OFF and display all points ON compound command
(21)	NOP	0	1	0	1	1	1	0	0	0	1	1	Command for non-operation
(22)	Test	0	1	0	1	1	1	1	*	*	*	*	Command for IC test. Do not use this command

(Note) *: disabled data

6. LED Backlight Specification



PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
FORWARD VOLTAGE	TEMPERATURE=+25°C FORWARD CURRENT=75mA	4.0	4.1	4.2	V
PEAK WAVE LENGTH	FORWARD CURRENT=75mA		568		nm
LUMINANCE	FORWARD CURRENT=75mA	10.0	13.0		cd/m2

LED COLOR: YELLOW-GREEN

NOTES: THE LUMINANCE IS THE AVERAGE VALUE OF 9 SAMPLE POINTS AND THE BACKLIGHT UNIFORMITY SHALL BE BETTER THAN 1.5 : 1
THE MEASUREMENT INSTRUMENT IS BM-7 LUMINANCE COLORIMETER. THE MEASURING DISTANCE IS 0.35M±5CM AND THE MEASURING FIELD IS 2°

▨ DOUBLE SIDE TAPE (3M 415). A

SILVER PAPER. (ADHESIVE BACK SIDE)

: CRITICAL DIMENSION
◇ : SPECIAL CHARACTERISTICS
+ : SAFETY CHARACTERISTICS

ISSUE	AMENDMENT	DATE
1	UPDATE LED INFORMATION	00-11-1
A	UPDATE DOUBLE SIDE TAPE	01.11.28

CONTROLLED
30 NOV 2001
VL DCC (CHINA) COPY

VL DCC (CHINA)

TITLE: BACK LIGHT (ASSEMBLY)
PROJECT NO: LCM075
TOLERANCE UNLESS OTHERWISE SPECIFIED: LINEAR : X.X ±0.2, X.XX ±0.1; ANGLE : 1.5°
DIMENSIONS IN MM
MATERIAL: PC
FINISH:
SCALE: DO NOT ON SCALE
THICKNESS:
THIRD ANGLE PROJECTION

	NAME	SIGN	DATE
DRAWN	WILSON CHOI		01.11.28
CHECKED	BILLY LAM		
APPROVED	ANDY LEUNG		

ITEM NO. LBL-LCM075-01B
DESCRIPTION: LCM075 BACK LIGHT LEDS2 YG
DWG NO: LBL-LCM075-01B REV 2
SHEET 1 OF 1